

# MARTIN CHAN

martinch@mit.edu · <https://martinchan.org/>

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## EDUCATION

### Massachusetts Institute of Technology (MIT)

(*In progress*) M.Eng in Computer Systems

Cambridge, MA

01/2024 – expected 06/2025

### Massachusetts Institute of Technology (MIT)

B.S. in Computer Science and Engineering · GPA: 4.6/5.0

Cambridge, MA

09/2019 – 06/2023

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## WORK EXPERIENCE

### MIT EECS, Head Teaching Assistant

Jan 2024 – May 2024

- Head TA for 6.192: Constructive Computer Architecture, an advanced undergraduate class on processor design and implementation with Prof. Arvind.
- Design and teach weekly recitation for 30 students.
- Give lectures when the professor is unavailable.
- Generally ensure the class runs smoothly (coordinate the undergraduate teaching assistants, manage assignments, etc.)

### MIT East Campus Dormitory, Mail Room and Front Desk Staff

Sep 2021 – May 2023

### MIT SHASS, Undergraduate Researcher

Summers 2020 and 2021

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## SELECTED PROJECTS

### Bluespec Language Server (*In Early Stages*) (<https://www.martinchan.org/blog/early-literature/>)

- Design and implement a language server (compiler-like) in Rust to support modern editor features (semantic highlighting, autocomplete, go-to-definition, hover for documentation, etc.) for writing Bluespec SystemVerilog HDL.
- Tool to be integrated into Visual Studio Code and other code editors through the Language Server Protocol.

### RISC-V Superscalar Processor (<https://martinchan.org/projects/processor/>)

- Improved my modest pipelined single-issue processor with magic memory into a superscalar processor with L1 caches, attempted out-of-order processing, branch prediction, prefetching, and optimized submodules.
- Wrote automated testing and logging infrastructure, instrumented processor to interface with official RISC-V tools, and integrated the Dhrystone benchmark.
- Tools used: Bluespec SystemVerilog, Konata, RISC-V software, RISC-V assembly, Bash and Python scripting.

### Bluespec SystemVerilog Extension for VS Code (<https://martinchan.org/projects/vscode-bsv/>)

- Wrote the only high-quality syntax highlighter for Bluespec available on Visual Studio Code. I published it on the VS Code extensions Marketplace for other Bluespec developers to use.
- I also wrote a separate high-quality lexer for syntax highlighting excerpts of Bluespec SystemVerilog on my website. I built the lexer using the open-source Rouge syntax highlighting engine.
- Tools used: Bluespec SystemVerilog, C preprocessor, TextMate grammar, Ruby Rouge, regular expressions.

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## SELECTED COURSEWORK

- Distributed Computer Systems Engineering
- Software Performance Engineering
- Multicore Programming
- Constructive Computer Architecture

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## LEADERSHIP

### East Campus Dormitory

*Fifth East Hall Chair*

MIT

Sep 2019 – Feb 2022

- Lead in dorm government and work with students, administrators, and faculty to address Institute policy, community issues, and building renovation. Three one-year terms.

### Institute Committee on Undergraduate Admissions and Financial Aid

*Committee Member*

MIT

Sep 2021 – May 2023

- Serve as one of three undergraduate members on the faculty committee responsible for formulating and reviewing policies on MIT undergraduate admissions and financial aid. Two one-year terms.

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## SKILLS

- **Programming languages:** *Proficient:* Go, Python, C, C++, Java, Bluespec SystemVerilog; *Intermediate:* Rust, SystemVerilog, Verilog
- Fluent in English (speak, read, write) and Cantonese (speak)

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## HOBBIES

Writing, cooking, woodworking, reading the *New Yorker*